SEETAL POTLURI

Postdoctoral Scholar
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Objective

To actively contribute to the hardware design, EDA, and security research and development, for cloud and edge accelerators.

Education

- 2009-2014: **Ph.D**, *Dept. of EE,* Indian Institute of Technology **(IIT)** Madras.
- 2007-2009: **M.Tech**, *Dept. of EE,* Indian Institute of Technology **(IIT)** Madras.
- 2003-2007: **B.Tech**, *Dept. of ECE, Amrita School of Engineering.*

Research Experience

- Mar. 2019 – Present: Postdoctoral Scholar, North Carolina State University.
- Jun. 2018 – Mar. 2019: Postdoctoral Scholar, Technical University of Dresden.
- Aug. 2016 – Jan. 2018: Senior DFT Engineer, Xilinx Asia Pacific, Singapore.
- Mar. 2015 – Aug. 2016: Postdoctoral Scholar, Technical University of Denmark.

Honors and Awards

- IEEE HOST Symposium 2021 – Best Paper Nominee.
- IEEE TTTC Doctoral Thesis Contest 2015 – Runner Up (Asia).
- Class topper with highest Cumulative G.P.A. during **M.Tech** as well as **B.Tech**.

Research Interests

Security, Reliability, Design-for-Test

Professional membership and participation

- Technical Program Committee Member
  - **IEEE Design Automation Conference** 2022
  - **IEEE Asia South Pacific Design Automation Conference** 2018, 2019, 2020, 2021, 2022
  - **IEEE European Test Symposium** 2016, 2017 and 2018
  - **IEEE Asian Test Symposium** 2017
- Session Co-Chair
  - **IEEE International Symposium on Circuits and Systems** 2020
  - **IEEE Design, Automation and Test in Europe** 2017
  - **IEEE Asian Test Symposium** 2017

Publication List

Google Scholar Profile: https://scholar.google.com.sg/citations?user=TG9epCwAAAAJ&hl=en

Selected Peer-Reviewed Conference Publications

- F. Aydin, E. Karabulut, **S. Potluri,** E. Alkim, and A. Aysu, “RevEAL: Single-Trace Side-Channel Leakage of the SEAL Homomorphic Encryption Library”, **IEEE Design, Automation, and Test in Europe (DATE)**, 2022 **(Accepted).**

- **S. Potluri,** and A. Aysu, “Stealing Neural Network Models through the Scan-Chain: A New Threat for ML Hardware”, **IEEE International Conference on Computer Aided Design (ICCAD)**, 2021 **(Accepted).**

- G. Haas, **S. Potluri,** and A. Aysu, “iTimed: Cache Attacks on the Apple A10 Fusion SoC”, **IEEE International Symposium on Hardware Oriented Security and Trust (HOST)**, 2021.

- **S. Potluri,** A. Aysu and A. Kumar, “SeqL: Secure Scan-Locking for IP Protection”, **IEEE International Symposium on Quality Electronic Design (ISQED),** 2020, pp. 7-13.

- F. Aydin, P. Kashyap, **S. Potluri,** P. Franzon and A. Aysu, “DeePar-SCA: Breaking Parallel Architectures of Lattice Cryptography via Learning Based Side-Channel Attacks”, **International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)**, 2020, pp. 262-280.

- F. Aydin, P. Kashyap, **S. Potluri,** P. Franzon and A. Aysu, “Breaking Side-Channel Countermeasures through Deep Learning”, **IEEE International Conference on Computer Aided Design (ICCAD)**, 2020 **(Invited).**

- Q. Tan, **S. Potluri** and A. Aysu, “Efficacy of Satisfiability-based Attacks in the Presence of Circuit Reverse-Engineering Errors”, **IEEE International Symposium on Circuits and Systems (ISCAS),** 2020, pp. 1-5.

- H. Chen, **S. Potluri** and F. Koushanfar, “FlowTrojan: Insertion and Detection of Hardware Trojans on Flow-Based Microfluidic Biochips”, **IEEE International New Circuits and Systems Conference (NEWCAS),** 2020, pp. 158-161.

- **S. Potluri,** A. Schneider, M. Horslev-Petersen, P. Pop and J. Madsen, “Synthesis of On-chip Control Circuits for mVLSI Biochips”, **IEEE/ACM Design Automation and Test in Europe (DATE),** 2017, pp. 1799-1804.

- **S. Potluri**, A. Mathew, R. Nerukonda, I. Hartanto and S. Toutounchi, “Cell-aware ATPG to improve defect coverage for FPGA IPs and next generation MPSoCs”, **IEEE Asian Test Symposium (ATS),** 2017, pp. 157-162**.**

- M. C. Ekesen, P. Pop and **S. Potluri**, “Architecture Synthesis of Cost Constrained Fault Tolerant Flow-based Biochips”, **IEEE/ACM Design Automation and Test in Europe (DATE)**, 2016, pp. 618-623.

- A. Satya Trinadh, S. G. Singh, Ch. Sobhan Babu, **S. Potluri** and V. Kamakoti, “DP- fill : A dynamic programming approach to X- filling for minimizing peak test power in scan tests", **IEEE/ACM Design Automation and Test in Europe (DATE)**, 2015, pp. 836-841.

- Huili Chen, **Seetal Potluri** and Farinaz Koushanfar, “BioChipWork: Reverse Engineering of Microfluidic Biochips”**, IEEE International Conference of Computer Design (ICCD),** 2017, pp. 9-16.

- **S. Potluri**, A. S. Trinadh, C. Rajamanikkam and S. Balachandran, “LPScan : An algorithm for supply scaling and switching activity minimization during test", **IEEE International Conference on Computer Design (ICCD)**, 2013, pp. 463-466.

- **S. Potluri,** A. S. Trinadh, S. Saraf and V. Kamakoti, “Component fault localization using switching current measurements”, **IEEE European Test Symposium (ETS),** 2016, pp. 1-2**.**

- **S. Potluri,** A. S. Trinadh, R. Baskaran, N. Chandrachoodan and V. Kamakoti, “PinPoint: An algorithm for enhancing diagnostic resolution using capture cycle power information”, **IEEE European Test Symposium (ETS),** 2013, pp. 1**.**

Selected Journal Articles

- **S. Potluri,** S. Kundu, A. Kumar, K. Basu and A. Aysu, “SeqL+: Secure Scan-Obfuscation with Theoretical and Empirical Validation”, **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Under Review).**

- P. Kashyap, F. Aydin, **S. Potluri,** P. Franzon and A. Aysu, "2Deep: Enhancing Side-Channel Attacks on Lattice-Based Key-Exchange via 2D Deep Learning"**, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 40, No. 6, pp. 1217-1229.

- H. Chen, **S. Potluri** and F. Koushanfar, "Security of Microfluidic Biochip: Practical Attacks and Countermeasures", **ACM Transactions on Design Automation of Electronic Systems (TODAES)** 2020, 27:1-27:29.

- G. V. Krishnan, V. Kamakoti, N. Chandrachoodan, **S. Potluri**, "A Scalable Pseudo-Exhaustive Methodology for Testing and Diagnosis in Flow-based Microfluidic Biochips", **IET Computers and Digital Techniques,** Vol. 14, No. 3, pp. 122-131.

- **S. Potluri,** P. Pop and J. Madsen, "Design-for-Testability of On-Chip Control in mVLSI Biochips", **IEEE Design and Test of Computers,** Vol. 36, No. 1, 2019, pp. 48-56.

- A. S. Trinadh, **S. Poturi,** Ch. Sobhan Babu, S. G. Singh and V. Kamakoti, "Optimal Don't Care Filling for Minimizing Peak Toggles During At-Speed Stuck-At Testing", **ACM Transactions On Design Automation of Electronic Systems (TODAES)**, Vol. 5, No. 1, 2017.

- **S. Potluri**, A. Satya Trinadh, Ch. Sobhan Babu, V. Kamakoti and N. Chandrachoodan, "DFT Assisted Techniques for Peak Power Reduction during Scan Tests", **ACM Transactions On Design Automation of Electronic Systems (TODAES)**, Vol. 21, No. 1, 2015.

- S. L. P. S. K. Patanjali, M. Patnaik, **S. Potluri** and V. Kamakoti, "MLTimer: Leakage Power Minimization in Digital Circuits Using Machine Learning and Adaptive Lazy Timing Analysis", **Journal of Low Power Electronics**, Vol. 14, No. 2, 2018, pp. 285-301.

- S. Burman, **S. Potluri,** D. Mukhopadhyay and V. Kamakoti, "Power Consumption Vs. Hardware Security: Feasibility Study of Differential Power Attack on Linear Feedback Shift Register Based Stream Ciphers and Its Countermeasures", **Journal of Low Power Electronics**, Vol. 12, No. 2, 2016, pp. 99-106.

- A. S. Trinadh, **S. Potluri, "**An Efficient Heuristic for Peak Capture Power Minimization During Scan-Based Test", **Journal of Low Power Electronics,** Vol. 9, No. 2, 2013, pp. 264-274.

- **S. Potluri,** N. Chandrachoodan and V. Kamakoti, "Interconnect Aware Test Power Reduction", **Journal of Low Power Electronics,** Vol. 8, No. 4, 2012, pp. 516-525.

- R. Pasumarthi, V. R. Devanathan, V. Vishvanathan, **S. Potluri** and V. Kamakoti, "Thermal-Safe Dynamic Test Scheduling Method Using On-Chip Temperature Sensors for 3D MPSoCs", **Journal of Low Power Electronics,** Vol. 8, No. 5, 2012, pp. 684-695.

Published Patents

S. Potluri, P. Pop and J. Madsen, "Complementary pneumatic digital logic for on-chip control of lab-on-chip devices", World Intellectual Property Organization (WIPO) 2018, Pub. No. **WO/2018/104516**.
Link: https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2018104516

Workshops Attended

- R. B. Carpi, "**Side Channel Analysis and Fault Injection",** Raleigh, North Carolina, March 2019.

- M. Witteman et al, **"Riscure User Workshop",** Fort Meade, Maryland, October 2019.